The above changes to the claims have been made to delete multiple dependency of the claims, to round out the scope of patent protection being sought, and generally to place the claims in better condition for examination on the merits. These changes have been made in accordance with 37 C.F.R. § 1.121 as amended on November 7, 2000.

Respectfully submitted,

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Marked-up Claims 4-10, 11-14, 16, 18-20, 22-24, 26-27, 32-33 and 35-38

4. (Amended) Apparatus as claimed in claim 1[, 2 or 3], wherein, latency tolerant modules connected to the secondary bus are arranged such that the least tolerant modules are located closer to the primary bus than the more tolerant modules.

5. (Amended) Apparatus as claimed in [any one of the preceding claims] claim 1, wherein the bus architecture has two or more secondary buses, each one connected to the primary bus via a separate primary to secondary interface module.

6. (Amended) Apparatus as claimed in [any one of claims 1 to 5] claim 1, wherein the primary bus comprises:

a write data bus for transferring write data between modules;

a read data bus for transferring read data between modules;

a transaction bus for transferring control data between modules,

the read data bus and the write data bus being physically separate from one another.

7. (Amended) Apparatus as claimed in [any one of claims 1 to 6] claim 1, wherein the secondary bus comprises:

a write data bus for transferring write data between modules;

a read data bus for transferring read data between modules;

a transaction bus for transferring control data between modules,

the read data bus and the write data bus being physically separate from one another.

8. (Amended) Apparatus as claimed in [claim 6 or 7] claim 6, wherein a read transaction by a master module involves placing read address data indicating the location of the required data on the transaction bus to which the master module is connected, and the master module receiving the required read data from a target module on the read data bus to which the master module is connected at an arbitrary time after the read address has been placed on the transaction bus, and wherein the write and transaction buses are available for use during reception by the master module of the return read data.

9. (Amended) Apparatus as claimed in [any one of the preceding claims] claim 6, further comprising:

means for assigning each module in the system one of a predetermined number of priority levels;

means for assigning each module an initial position within a queue;

means for receiving respective transaction requests from modules;

means for filtering the transaction requests from the modules so as to retain the requests from those modules having the highest priority level of the modules making such requests, thereby producing a set of filtered requests;

means for selecting from the set of filtered requests, the transaction request from the module having the highest position within the queue, and

means for sending a request grant message to the module from which the selected transaction request was received.

11. (Amended) Apparatus as claimed in claim 9 [or 10], comprising means to place a module receiving a transaction grant message at the bottom of the queue.

12. (Amended) Apparatus as claimed in [any one of the preceding claims] claim 1, further comprising:

a first arbiter means for controlling initiating transactions on the bus architecture; and

a second arbiter means for controlling return transactions on the bus architecture.

13. (Amended) Apparatus as claimed in claim 12, [when read as dependent upon claim 5 or 6,] wherein the first arbiter means controls use of the write and transaction buses and the second arbiter means controls use of the read bus.

14. (Amended) Apparatus as claimed in [any one of the preceding claims] claim 12, wherein each module is assigned an address range in a memory map of the apparatus, and wherein the apparatus further comprises;

reception means for receiving and storing availability data indicative of the availability of modules;

transaction request means for producing a transaction request including target address data indicating a target location in the memory map for the transaction;

decoding means for decoding the target address data to produce identity data relating to a target module, the target module being assigned an address range in the memory map which includes the target address data;

comparison means for analysing the stored availability data corresponding to the target module identified by the identity data; and

transaction means, responsive to the comparison means, for terminating the transaction request if the analyzed availability data indicates that the target module is unavailable.

16. (Amended) Apparatus as claimed in [any one of the preceding claims] claim 14, comprising:

means for receiving data requests from modules for respective required data packets, each request including address data indicating the location of the data packet concerned, and sequence data indicating the timing of the request relative to other data requests;

means for receiving returned data packets and associated sequence data;

a storage device for storing the returned data packets in respective storage locations therein, in the order indicated by the associated sequence data; and

retrieval means for retrieving data packets from the storage device in the order of the storage locations of the storage device.

18. (Amended) Apparatus as claimed in claim 16 [or 17], wherein the storage device is provided by a dual port RAM device.

19. (Amended) Apparatus as claimed in [any one of the preceding claims] claim 16, comprising:

a storage device;

means for receiving read transaction requests from modules, each request including address data indicating the location of the data to be retrieved, and identity data indicating the source of the transaction message;

means for sending the address data to the storage device;

means for storing the identity data in a queue;

means for receiving a retrieved data item from the storage device;

means for matching the retrieved data item with the identity data at the front of the queue; and

means for returning the retrieved data to the module identified by the matched identity data.

20. (Amended) Apparatus as claimed in [any one of the preceding claims] claim 1, comprising:

an arbitration unit for granting access to the bus in response to requests received from the modules, the granting of access being in the form of a dedicated data packet issued from the arbitration unit, whereby only the module which has been granted access can use that particular dedicated packet to gain access to the bus;

wherein the arbitration unit is operable to issue empty data packets during periods when the bus is idle, the empty data packets being usable by a module to gain access to the bus without making a specific request to the arbitration unit for a dedicated packet.

22. (Amended) Apparatus as claimed in claim 20 [or 21], wherein each module has means for converting a dedicated packet intended for itself into an empty packet.

23. (Amended) Apparatus as claimed in claim 20[, 21 or 22], wherein the arbitration unit is located at one end of the bus.

24. (Amended) Apparatus as claimed in [any one of the preceding claims] claim 20, wherein the or each bus comprises:

a plurality of bus connection units for connecting modules to the bus concerned; and

a plurality of bus portions arranged in series, each bus portion, except the last in the series, being connected to the next portion in the series by way of a bus portion connection unit.

26. (Amended) Apparatus as claimed in claim 24 [or 25], wherein each bus connection unit includes output circuitry connected to the bus portions to which the unit is connected, the output circuitry being optimised for the length of the bus portions concerned.

27. (Amended) Apparatus as claimed in claim 24[, 25 or 26], wherein the bus portions are all substantially equal in length.

32. (Amended) Apparatus as claimed in claim 30 [or 31], wherein each module has means for converting a dedicated packet intended for itself into an empty packet.

33. Apparatus as claimed in claim 30[, 31 or 32], wherein the arbitration unit is located at one end of the bus.

35. A computer system comprising apparatus as claimed in [any one of the preceding claims] claim 34.

36. An integrated circuit comprising apparatus as claimed [in any one of the preceding claims] claim 34.

37. A graphics processing system comprising apparatus as claimed [in any one of the preceding claims] claim 34.

38. A games console comprising apparatus as claimed [in any one of the preceding claims] claim 34.